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TRANSFORMER ISOLATED BUCK-BOOST CONVERTERS

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Abstract **-** Of the single-switch dc-to-dc converters, those with the buck-boost voltage transfer function offer the best potential for transformer coupling, hence isolation, at the kilowatt level. This paper highlights the limitations of the traditional magnetic coupled, buck-boost topology. Then four split-capacitor transformer-coupled topologies (specifically the Cuk, sepic, zeta, and new converters) with a common ac equivalent circuit, that do not temporarily store core magnetic energy as does the traditional isolated buck-boost converter nor have a core dc magnetizing current bias as with the sepic and zeta transformer coupled topologies, are explored. Core dc bias capacitive voltage compensation is a practical design constraint in three of the four topologies, while all four must cater for stray and leakage inductance effects. Simulations and experimental results for the new converter at 408W that support the transformer-coupled, single-switch dc-to-dc converter concepts are investigated.

Keywords **-** switched mode power supplies, smps, dc-to-dc converters, buck boost converters, transformer isolated buck boost converters, Cuk converter, sepic converter, zeta converter, inverse sepic converter.

I. INTRODUCTION

DC-to-dc converters are the enabling backbone of virtually all electronic systems, in industrial, consumer, and domestic products, like hand-held and portable electronics, and every computer. For safety, insulation, compatibility, and noise reasons, most applications require electrical isolation of the converter output from the energy source, where the transformer coupled flyback converter is a viable solution up to a few hundred watts. But higher power electrical isolation may be required by electric vehicles [1], battery chargers [2], fuel cell [3], [4], solar [5], [6], and wind energy, involving super-capacitors, smart grids and distributed generation [7], [8], electronic ballast [9], energy harvesting [10], and power factor correction [11], to name just a few application areas.

Various techniques are used to increase the power capabilities of the basic converters, including interleaved or multiphase converters, bidirectional dc-to-dc converters [12], [13], multiple input converters [14], cascaded output converters, high voltage supplies [15], [16], snubbers [17], and various control techniques [18]-[21]. Flyback circuits use an extra winding, namely a catch winding, and suffer from leakage effects and duty cycle limitations to ensure magnetic core flux reset. Eventually, electrical operating levels are reached where multiple switch topologies are used, like the push-pull converter or variations of the half and full H-bridge converters, where better utilization of the magnetic core is gained by high frequency balanced operation alternating between two magnetic B-H quadrants. Such techniques, although viable, require multiple switches and may resort to the complication of resonant techniques or passive and active snubbers to contain switch losses at ever increasing operating frequencies and through-put power levels.

The basic buck-boost converter output can be isolated via a coupled magnetic circuit [22]. Additional features to isolation are voltage matching and better semiconductor utilization, but the limitation is that magnetic energy is temporarily stored in the coupled circuit core. Thus for a given magnetic material, maximum energy transfer is restricted by core volume, viz. *½BH*× Volume.

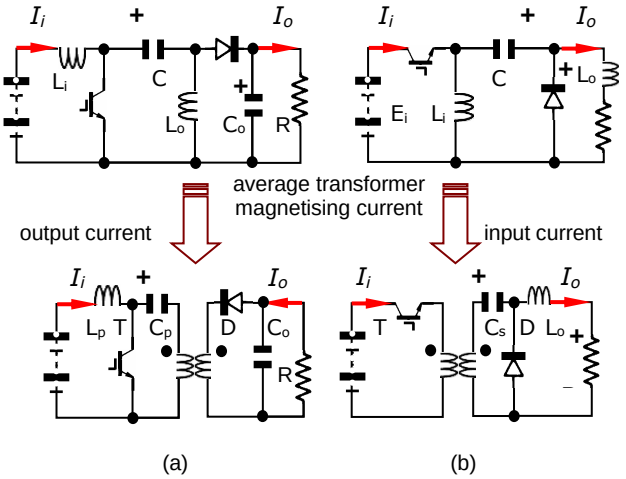

Fig .1. Inductor coupled circuit magnetizing dc bias current of (a) sepic and (b) zeta converters.

The core volume is utilized more effectively if magnetic energy transfer is through instantaneous transformer action rather than transfer with intermediate magnetic energy storage. The transformer coupling method commonly used for the sepic and zeta converters are shown in Figure 1, but these topologies result in a core dc flux bias attributable to the output and input average currents, respectively. A better approach is the split-capacitor transformer-coupled Cuk converter topology that utilizes the transformer transfer mechanism criteria without a dc flux bias. This paper identifies three further topologies, all with buck-boost transfer functions, that can operate in a transformer coupled mode, without a dc flux bias. As well as the Cuk converter, the other topologies are based on the sepic and zeta converters, with the fourth topology previously unidentified. Importantly, the common coupling of the circuit inductor in the sepic and zeta converter cases in Figure 1 is not that proposed in this paper, nor is the approach, the intermediate storage approach, used with the common buck-boost isolated converter. The split capacitor ac-mirroring approach adopted with the Cuk converter is employed in all four cases. The four considered topologies represent the four possibilities yielded from two possible transformer primary stage arrangements together with two possible transformer secondary circuit arrangements. A transformer allows all four converters to have the same buck-boost output polarity. The operating similarities and mechanisms of each of the four converters are evaluated and supported by time domain simulations and experimentation. No catch winding, as with a flyback converter, is used.

II. TRANSFORMER ISOLATED BUCK-BOOST CONVERTERS

The conventional isolated buck-boost converter, termed topology A5 in Table I, operates by temporarily storing energy, $\frac{1}{2}BH\times$Volume, in the magnetic core volume. The core volume is utilized differently if electrical energy transfer is through magnetic transformer action rather than core intermediate energy storage. If converter energy is transferred from the source to the load via ripple current (energy change) through a series capacitor, as in Figure 2(a), then that capacitor can be split so as to facilitate an interposed high magnetizing inductance shunt current transformer, as shown in Figure 2(b), and as with the Cuk converter, topology C5 in Table 1. AC-wise, if the output in Figure 2 is to be the same in both circuits, the secondary capacitor must electrically mirror the primary capacitor, so both are equal valued, if the transformer turns ratio $N_s/N_p = \eta_T$ is unity. The secondary capacitor is needed for supporting any dc bias associated with the secondary dc circuit conditions.

The common approach with the sepic and zeta converters is to replace a circuit inductor with a magnetically coupled inductor, as in Figure 1. Although its average voltages are zero, the core has an mmf bias (hence flux bias) due to a dc bias current component, which necessitates an air gap which adversely reduces the magnetizing inductance. The dc current bias, which is a maximum at full load, significantly decreases the allowable alternating flux and increases copper I^2R losses due to the increased number of turns. However, an air gap reduces coupling, which increases leakage inductance, with the associated store energy stressing the converter switch at turn off. Such coupling through circuit inductance can be summarized as a mechanism that requires enhancement of magnetic core imperfections (air gap increased mmf before current saturation onset), whilst split-capacitor transformer coupling relies on magnetic circuit perfection (infinite transformer magnetizing inductance).

A transformer offers voltage matching, hence better semiconductor device utilization by turns ratio variation (semiconductor duty cycle can be increased so as to decrease semiconductor peak current). Secondary circuit reactance can be transferred to the primary for ac analysis according to the turns ratio, squared.

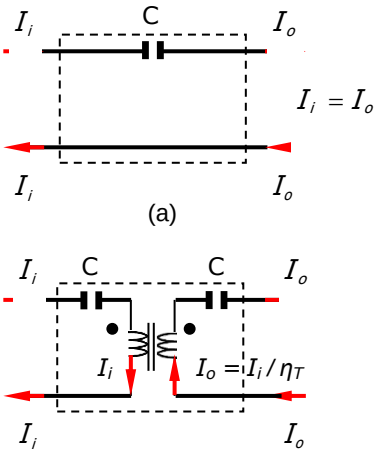

Fig .2. Capacitor ac circuit models:(a) series capacitor ac model and (b) equivalent ac capacitor model using transformer coupling.

Examination of the thirty-three known single-switch, single-diode, dc-to-dc converters [23] reveals that the

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Cuk C5, sepic G6, zeta G5, and new buck-boost P5 converters, as shown in Table 1, all with a buck-boost magnitude transfer function, fulfill the series energy transfer capacitor requirement, shown in Figure 2(a). Although the transformer plus split-capacitor buffering approach is commonly used to isolate the Cuk converter output, its possible use on the sepic and zeta converters [24] has been virtually unexploited, with the coupled magnetic circuit with flux bias replacement of an inductor approach favored for these two converters, as in Figure 1. Both references [23] and [24] (c.f. Figure 11(b)) preclude the proposed new buck-boost topology P5, considered as being degenerate. However, with a dc-to-dc switched mode converter, energy transfer is ac circuit based (inductor current variation), while the transfer function is a dc level mechanism (average inductor current). Thus, analysis degeneracy only defines its transfer function, obliterating and masking any unique practical dc circuit features of the pre-degenerate topology. The independence of ac and dc circuit operating mechanisms and their superposition properties should be appreciated. This independence is illustrated by considering the inductor ac and dc currents in any of the basic three dc-to-dc converters. For a given duty cycle (output voltage), as the load is varied, the dc current in the inductor varies, but the superimposed ripple current magnitude remains the same. Conversely, the ripple current magnitude changes with duty cycle, as does the output voltage, yet the load can be adjusted to maintain a constant superimposed inductor, hence constant load and current.

All four converters (in fact all five in Table 1) are reversible (using two switch-diode anti-parallel connected pairs). The sepic G5 and zeta G6 converters are the reverse (or inverse) of each other, while due to circuit symmetry, the other two converters, Cuk C5 and P5, reverse to be the original topology.

Figure 3 shows how the one circuit topology can realize the four considered capacitor-coupled converter topologies in Table 1, by the appropriate reconnection of one end of each transformer winding. Conveniently, the switch emitter is at the zero volt level for all four converters. The ac equivalent circuit of each converter is the same, while the dc equivalent circuits only differ with the mirroring capacitors being dc voltage biased by the input and/or output voltages. The relative input and output voltage polarities remain fixed, as shown in Figure 3. The interposed shunt transformer acts in an ac current controlled mode where the voltage adjusts to meet the corresponding voltage requirement associated with the transformer equation ($I_p / I_s = V_s / V_p = N_s / N_p$), along with the converter current/voltage transfer function ($I_i / I_o = V_o / E_i = |\delta / (1-\delta)|$); both enforced since both equations comply with energy conservation. Because of the ac equivalent circuit similarities of the four converters, their component and operational design (including discontinuous conduction operation) and closed loop control design and performance, are all similar. Therefore, because of extensive pre existing research into Cuk, sepic, and zeta converter closed loop operation, such aspects need not be considered in this paper.

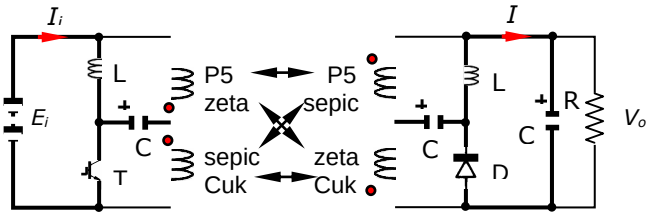

Fig .2. Four converters from a single circuit topology, with dot convention for each are shown, but reverse mode switch and diode are not shown..

III. TRANSFORMER/CAPACITOR DC BLOCKING

In the Cuk, sepic and zeta converter cases, the split-capacitor mirroring pair in Figure 2(a) must fulfill the important function of buffering, specifically blocking, a dc voltage component from the magnetic coupling element. Table 1 shows the dc component (the input and/or output voltage) each of the series split capacitors, C_p and C_s, must block, hence support. However, the split capacitors, the Cuk converter, C5, potentially experiences an additive dc component on both windings (E_i, V_o), while the sepic G5 (E_i, 0) and zeta G6 (0, V_o) converters potentially only experience dc voltage on one winding (primary and secondary, respectively). The dc voltage component is catered for and blocked, by using large capacitance, thereby preventing core saturation. Thus, in these three converters the series split capacitors serve a dual purpose, namely part of the ac energy transfer mechanism (usually associated with high ripple current) and dc voltage blocking. The new buck-boost converter P5 develops no potential dc

voltage component on the primary or the secondary, because each winding is in parallel with inductance, which as for the zeta converter primary and sepic converter secondary, supports zero average voltage. In practice, in all four converter cases, any capacitor dc voltage bias is accentuated due to circuit non-ideal component voltage drops, including semiconductor, inductor and transformer winding resistance associated (current dependant) voltages. Large capacitance is therefore not necessary for the new converter P5 and such coupling is not applicable to the degenerate basic buck-boost converter A5 if transformer non-storage energy action is to be exploited.

IV. OPERATIONAL CONSTRAINTS

Because all five considered topologies have the same ac equivalent circuit (s/c dc supplies etc.), the switch, diode and inductor peak and average ratings are the same for all five, as are the capacitor ac characteristics for the four split-capacitor topologies. These common electrical characteristics are summarized in table 2. In each case, the average current in the input side (primary) and output side (secondary) inductors, L_p and L_s, are the input and output average currents, I_i and I_o, respectively. Only capacitor dc voltage ratings differ, as shown in Table 1. For analysis expediency, the transformer turns ratio is assumed unity ($\eta_T = 1$) and the dc blocking capacitors are assumed equal ($C_p = C_s = C$). Consequently, both capacitor ac voltages and ac currents mirror each other.

With an inductor in the transformer winding Kirchhoff voltage loop, the average winding voltage is zero, as is the case for one side of the transformer in the zeta (the primary) and sepic (the secondary) converters, and for both sides in topology P5. Since the capacitor on the zero average-voltage-side does not need significant dc blocking capability, the capacitance is dimensioned based solely on circuit ac voltage and frequency restrictions (as opposed to average voltage values plus a superimposed ripple component).

In each of the four transformer action coupled cases, circuit functionality requires that the input and output inductor currents are continuous. Specifically with a continuous conduction mode, CCM, the transfer function integrity and in particular the transformer volt-second (per turn) zero balance is maintained according to the average inductor current, and is not affected by the ripple current magnitude. Inductor ripple current magnitude only influences the minimum load, that is, the CCM-DCM (discontinuous conduction mode) boundary. Non-linear DCM operation is viable, without core saturation, since the magnetizing current falls to zero every cycle.

Energy is transferred in a single direction through the transformer: winding voltage polarities change depending on whether the capacitors are charging or discharging, but with zero average capacitor current.

Capacitance transfers between transformer sides in the turns ratio, inverse squared ($X_c \propto 1/C$). Thus in preserving equal energy change for both capacitors, with a turns ratio $N_s / N_p = \eta_T$, capacitance can be varied, with the voltage satisfying

$$V_o = \eta_T E_i \frac{\delta}{1-\delta} \qquad (1)$$

where the switch T is on, t_{on} and T is off, t_{off}, (such that $t_{on} + t_{off} = \tau = 1/f_s$ where f_s is the switching frequency) giving the switch on-state duty cycle as $\delta = t_{on} / \tau$.

- Capacitors, C_p and Cs

Decreasing split capacitance increases capacitor ripple voltage, but does not necessarily influence the CCM/DCM boundary. The ripple voltage peak-to-peak magnitude is independent of the capacitor dc bias level and is given by

$$\Delta V_{Cp} = (1-\delta)\frac{I_i \tau}{C_p} = \delta \frac{I_o \tau}{C_p} \qquad (2)$$

$$\Delta V_{Cs} = \delta \frac{I_o \tau}{C_s} = (1-\delta)\frac{I_i \tau}{C_s} \qquad (3)$$

Capacitor ripple voltage is independent of inductances L_p and L_s, and for unity turns ratio $\eta_T = 1$:

$$\Delta V_{Cp} = \Delta V_{Cs} \text{ if } C_p = C_s$$

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Table 1. Five Buck-boost Topologies, Showing Inserted Transformer and Split-capacitor Theoretical dc Voltage Stress Levels in Four Cases.

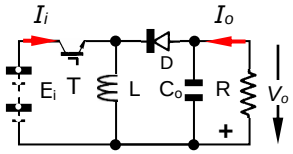
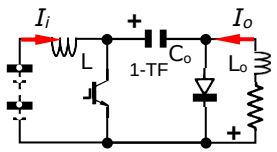
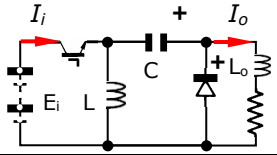
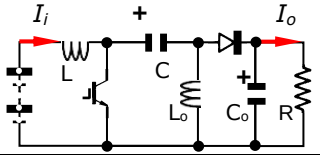
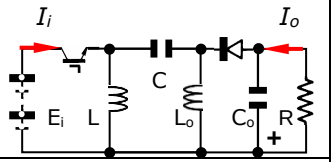
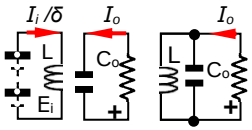
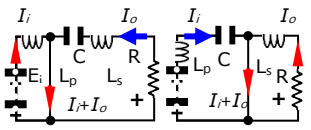
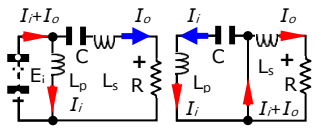
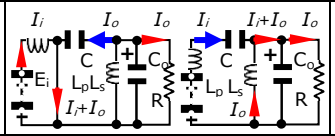
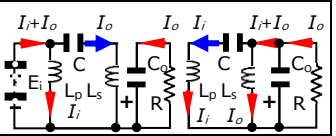
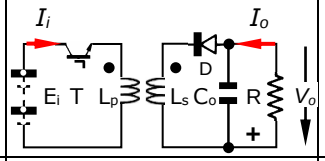
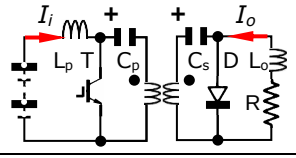
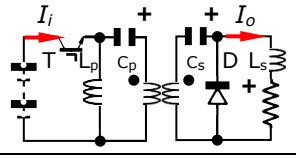
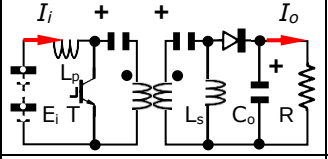
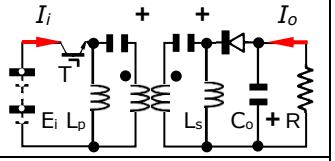
voltage sourced converters					
switch T state	switch T ON / switch T OFF	switch T ON / switch T OFF	switch T ON / switch T OFF	switch T ON / switch T OFF	switch T ON / switch T OFF
Two operating states					
Loop equations	$L\times\Delta i_L=\int v_L dt = t_{on}\times E_i = -t_{off}\times V_o$	$C\times\Delta v_c=\int i_c\,dt = -t_{on}\times I_o = t_{off}\times I_i$	$C\times\Delta v_c=\int i_c\,dt = t_{on}\times I_o = t_{off}\times I_i$	$C\times\Delta v_c=\int i_c\,dt = -t_{on}\times I_o = -t_{off}\times I_i$	$C\times\Delta v_c=\int i_c\,dt = t_{on}\times I_o = -t_{off}\times I_i$
Average capacitor voltage	-	$E_i + \lvert V_o\rvert$	V_o	E_i	**0**
Classification $\delta = t_{on}/\tau$ voltage transfer function $f_v(\delta)$	**A5** BUCK-BOOST (**a**) $-\frac{\delta}{1-\delta}$	**C5** Cuk (**b**) $-\frac{\delta}{1-\delta}$	**G6** ZETA (**c**) $+\frac{\delta}{1-\delta}$	**G5** SEPIC (**d**) $+\frac{\delta}{1-\delta}$	**P5** NEW (**e**) $-\frac{\delta}{1-\delta}$
features	Discontinuous input current voltage source output	Continuous input and output current	Discontinuous input current Continuous output current	Continuous input current voltage source output	Discontinuous input current voltage source output
Magnetic coupling (1:1 and C_p=C_s)					
Coupling mechanism	*Magnetic storage coupling*	*Transformer coupling*	*Transformer coupling*	*Transformer coupling*	*Transformer coupling*
Primary dc bias	I_i	E_i	**0**	E_i	**0**
Secondary dc bias	$I_i(1-\delta)/\delta$	V_o	V_o	**0**	**0**

Table 2. Common Component Characteristics.

$\delta = t_{on} / T = t_{on} f_s$	$\eta_T \left\lvert \frac{\delta}{1-\delta} \right\rvert$	Buck-boost converters	
$\eta_T = N_s / N_p = 1$		single inductor	two inductors
$C_p = C_s$	topology	A5	C5, G6, G5, P5
average voltage switch and diode	V_T , V_D	E_i , V_o	E_i , V_o
maximum voltage switch and diode	V_T , V_D	$E_i + V_o$, $E_i + V_o$	$E_i + V_o$, $E_i + V_o$
switch current average and peak	I_T , I_T	I_o δ/ 1-δ , I_o / 1-δ	I_o δ/ 1-δ, I_o / 1-δ
diode current average and peak	I_D , I_D	I_o , I_o / 1-δ	I_o , I_o / 1-δ
average inductor current input and output	$I_{Lp,}$, I_{Ls}	I_i / δ	I_i , I_o
inductor ripple current input and output	$\Delta I_{Lp} = \Delta I_{Ls}$	$\delta E_i T / L$	$\delta E_i T / L_p$, 1-δ $V_o T / L_s$
capacitor ripple voltage	$\Delta v_{Cp} = \Delta v_{Cs}$	--	$\delta I_o T / C$

Capacitor maximum *dv/dt* stress depends on the smaller of t_{on} and t_{off}, that is the duty cycle δ: when $\delta <$ ½ the maximum *dv/dt* stress is

$$\left.\frac{\Delta V_{Cp}}{\Delta t}\right|_{max} = \frac{I_o}{C_p} \quad \text{and} \quad \left.\frac{\Delta V_{Cs}}{\Delta t}\right|_{max} = \frac{I_o}{C_s} \tag{4}$$

when $\delta <$ ½ the maximum *dv/dt* stress is

$$\left.\frac{\Delta V_{Cp}}{\Delta t}\right|_{max} = \frac{I_i}{C_p} \quad \text{and} \quad \left.\frac{\Delta V_{Cs}}{\Delta t}\right|_{max} = \frac{I_i}{C_s} \tag{5}$$

The capacitor dc bias voltage is the input and/or output voltage, or zero, depending on the dc topology. If dc biased, the capacitor voltage reaches zero during the off-period (hence DCM) when:

from equation (2), for the primary side capacitor biased by E_i

$$I_i = 2\frac{E_i}{(1-\delta)\tau} C_p = 2\frac{V_o}{\delta\tau} C_p \tag{6}$$

corresponding to a critical minimum load resistance of

$$R_{DCM} < ½ \frac{\tau\delta^2}{C_p(1-\delta)} \tag{7}$$

from equation (3), for the secondary side capacitor biased by V_o

$$I_o = 2\frac{V_o}{\delta\tau} C_s = 2\frac{E_i}{(1-\delta)\tau} C_s \tag{8}$$

corresponding to a critical minimum load resistance of

$$R_{DCM} < ½ \frac{\tau\delta}{C_s} \tag{9}$$

Hence C5 has two capacitor discontinuous constraints, the zeta and sepic converters one capacitor constraint, while P5 has no capacitor constraints because of the juxtaposition of two inductors, L_p and L_s. Since the input and output currents are related by the transfer function, in the case of a non-reversible Cuk C5 converter, with η_T =1, both capacitors enter DCM simultaneously at a specific duty cycle, when

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$$C_p = \frac{\delta}{1-\delta} C_s \qquad (10)$$

- Inductors, L_p and L_s

DCM also occurs when an inductor current ripple reaches zero during the switch off period t_{off}, at which instant the associated capacitor maintains a constant dc bias voltage for the remainder of the switching period τ.

In each case, the primary-side inductor L_p average current is the average input current I_i, while the secondary-side inductor L_s average current is the output average current I_o. Operation assumes that both inductor currents are not discontinuous. The (current hence voltage) transfer function integrity is based on the average inductor current, independent of the ripple current magnitude. The ripple current specifies a DCM boundary, thus two CCM-DCM boundaries exist, viz. one for each inductor, L_p and L_s. The optimum design is the case where both inductors enter the discontinuous current mode at the same load current level, but unexploitably, this is only possible for a specific duty cycle.

For a given set of operating conditions and circuit component values, the input inductor L_p ripple current is the same for all four topologies, since each experiences the input voltage E_i for the same period of time t_{on}, that is

$$\Delta i_{Lp} = \frac{E_i t_{on}}{L_p} = \delta \frac{\tau E_i}{L_p} = (1-\delta)\frac{\tau V_o}{L_p} \qquad (11)$$

Similarly, for each topology, the output inductor L_s ripple current is the same in all four cases and can be expressed in terms of the output voltage V_o and switch off time t_{off}, specifically

$$\Delta i_{Ls} = \frac{V_o t_{off}}{L_s} = (1-\delta)\frac{\tau V_o}{L_s} = \delta \eta_T \frac{\tau E_i}{L_s} \qquad (12)$$

Inductor ripple current is independent of split capacitance C_p and C_s, and for unity turns ratio $\eta_T = 1$:

$$\Delta i_{Lp} = \Delta i_{Ls} \text{ if } L_p = L_s$$

Since the output inductor average current is equal to the load current and all four converters have the same output inductor ripple, the critical maximum load resistance R_{crit} for DCM is the same and can be determined from equation (12), as

$$R_{DCM} > \frac{2L_s}{(1-\delta)\tau} \qquad (13)$$

or if the input inductor enters discontinuous conduction before the output inductor, from equation (11)

$$R_{DCM} > \frac{2\delta L_p}{\tau(1-\delta)^2} \qquad (14)$$

Equating (13) and (14) gives the boundary condition as to which inductor enters DCM first, and like the capacitor DCM condition, is purely duty cycle dependant:

$$L_s = \frac{\delta}{1-\delta} L_p$$

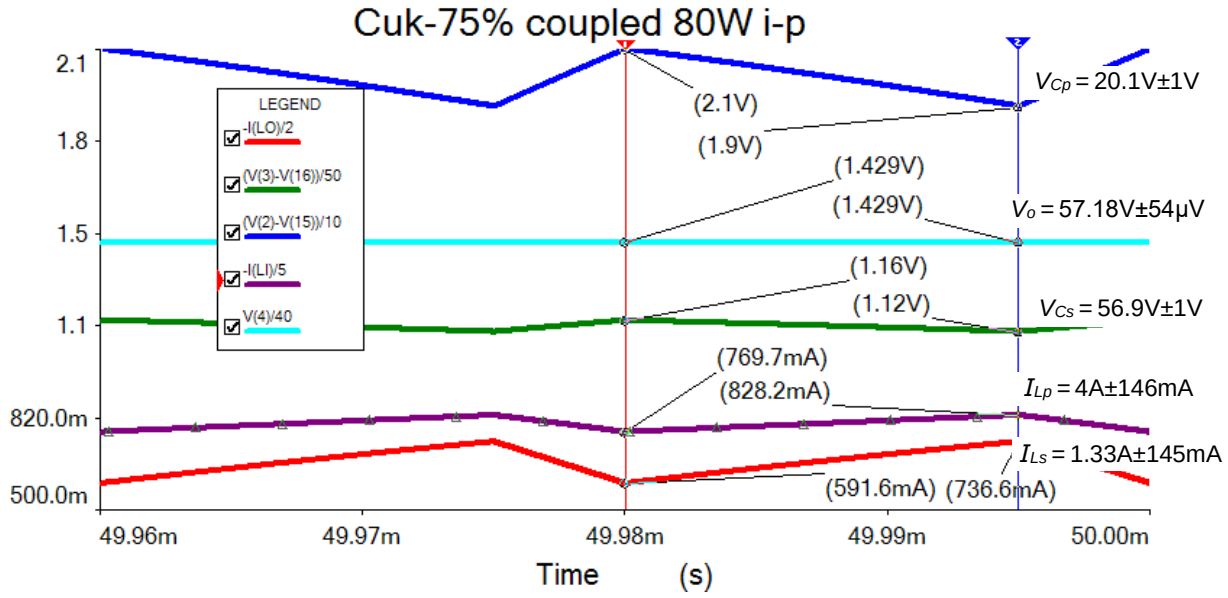
The ripple current (voltage) magnitude, hence inductance (capacitance), trades rapid response with large ripple current (voltage) against closed loop stability reduction and a higher DCM boundary.

V. CONVERTER SIMULATIONS

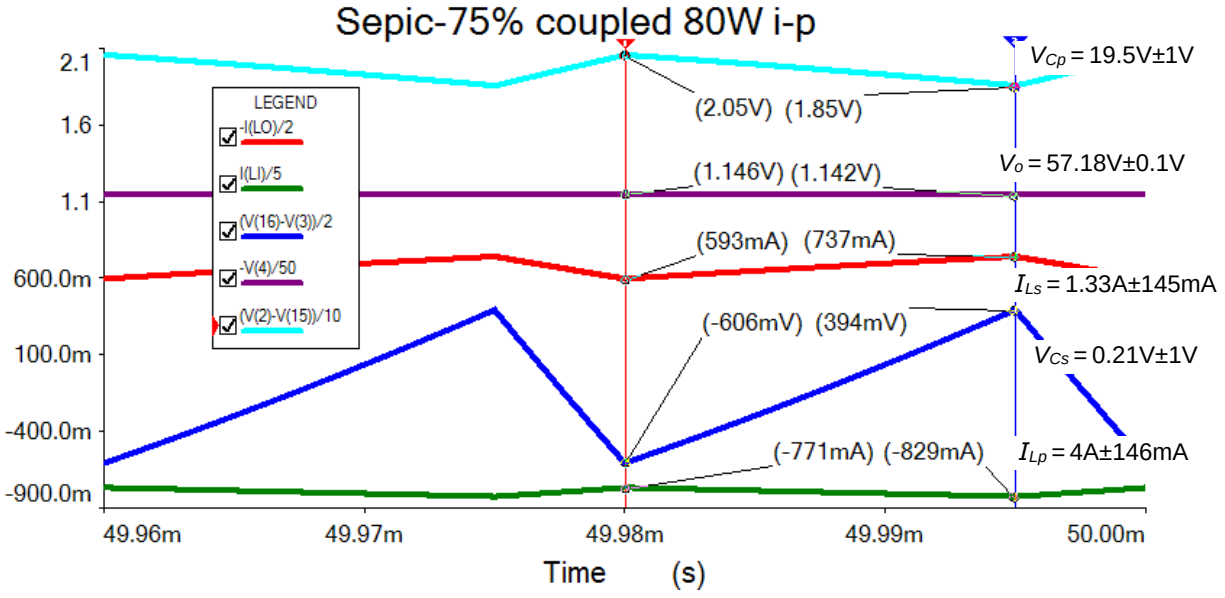
Table 3 summaries the component values used for the time domain transient simulations (and practically), with typical simulation results for each converter shown in Figure 4. Perfect transformer coupling, k =1, is assumed, with the practical consequences and remedies for leakage effects considered in subsequent sections.

Table 3. Component Values

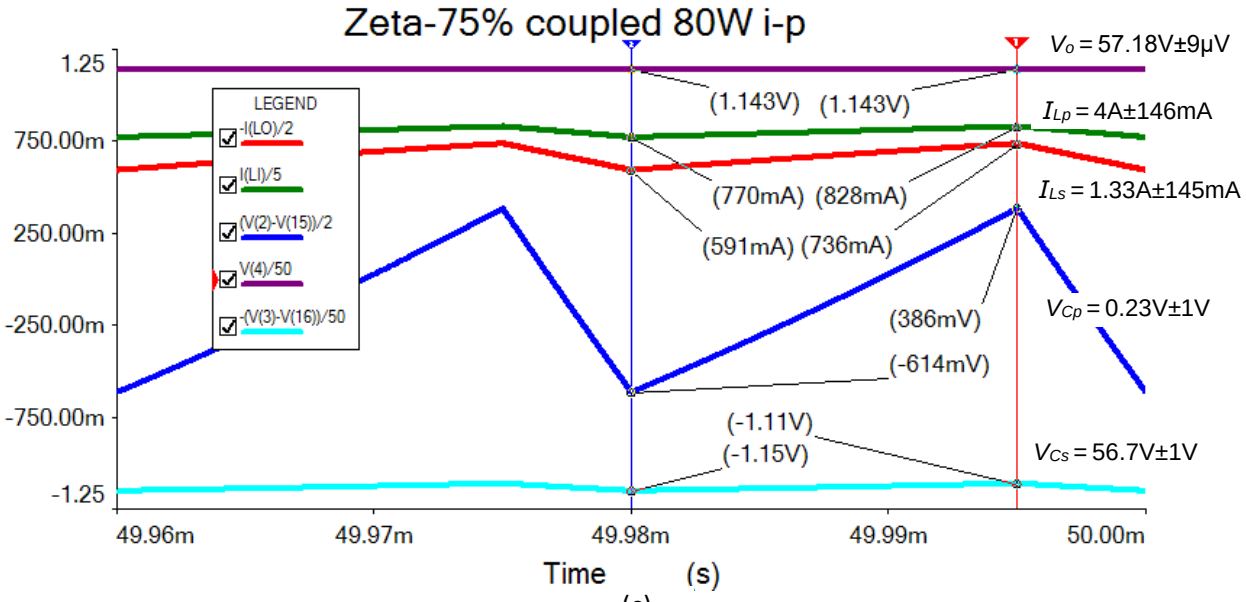
E_i	20V	T, mosfet	200V, 54mΩ
L_p	1.0mH, 74mΩ, 10A	D, SiC	600V, 10A
L_s	1.0mH, 74mΩ, 10A	t_{on}	15μs
C_p C_s	10μF, 10μF	Δ	75%
C_o	100μF	f_s	50kHz
η_T	1 (100mH:100mH)	K	1


Cuk-75% coupled 80W i-p
LEGEND
-I(LO)/2
(V(3)-V(16))/50
(V(2)-V(15))/10
-I(LI)/5
V(4)/40
2.1
1.8
1.5
1.1
820.0m
500.0m
(2.1V)
(1.9V)
(1.429V)
(1.429V)
(1.16V)
(1.12V)
(769.7mA)
(828.2mA)
(591.6mA)
(736.6mA)
V_{Cp} = 20.1V±1V
V_o = 57.18V±54µV
V_{Cs} = 56.9V±1V
I_{Lp} = 4A±146mA
I_{Ls} = 1.33A±145mA
49.96m
49.97m
49.98m
49.99m
50.00m
Time (s)

(a)


Sepic-75% coupled 80W i-p
LEGEND
-I(LO)/2
I(LI)/5
(V(16)-V(3))/2
-V(4)/50
(V(2)-V(15))/10
2.1
1.6
1.1
600.0m
100.0m
-400.0m
-900.0m
(2.05V) (1.85V)
(1.146V) (1.142V)
(593mA) (737mA)
(-606mV) (394mV)
(-771mA) (-829mA)
V_{Cp} = 19.5V±1V
V_o = 57.18V±0.1V
I_{Ls} = 1.33A±145mA
V_{Cs} = 0.21V±1V
I_{Lp} = 4A±146mA
49.96m
49.97m
49.98m
49.99m
50.00m
Time (s)

(b)


Zeta-75% coupled 80W i-p
LEGEND
-I(LO)/2
I(LI)/5
(V(2)-V(15))/2
V(4)/50
-(V(3)-V(16))/50
1.25
750.00m
250.00m
-250.00m
-750.00m
-1.25
(1.143V) (1.143V)
(770mA) (828mA)
(591mA) (736mA)
(386mV)
(-614mV)
(-1.11V)
(-1.15V)
V_o = 57.18V±9µV
I_{Lp} = 4A±146mA
I_{Ls} = 1.33A±145mA
V_{Cp} = 0.23V±1V
V_{Cs} = 56.7V±1V
49.96m
49.97m
49.98m
49.99m
50.00m
Time (s)

(c)

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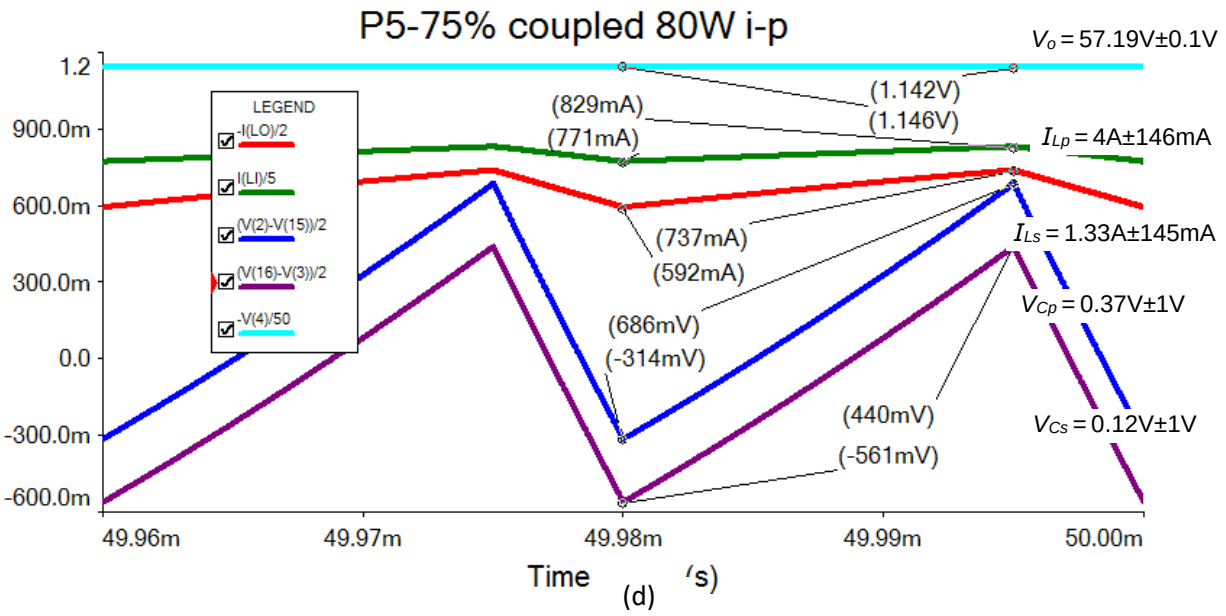

Fig .4. Simulation results at 20Vdc, 80W input, with δ=¾:(a) Cuk - C5, (b) sepic - G5, (c) zeta - G6, and (d) new - P5, converters.

Table 4. Simulation Results for the Four Transformer Coupled buck-boost Converters.

E_i = 20V δ=¾ R_o = 49.2Ω		Cuk	sepic	zeta	New
topology		C5	G5	G6	P5
ave I_i	A	4.00	4.00	4.00	4.00
P_{in}	W	79.90	80.00	79.91	80.01
ave $I_{Lp} \pm \Delta I_{Lp}$	A	4.00 ± 146m	4.00 ± 146m	4.00 ± 146m	4.00 ± 146m
ave $V_{Cp} \pm \Delta V_{Cp}$	V	20.1 ± 996m	19.54 ± 998m	0.23 ± 1.00	0.373 ± 1.00
ave $V_{Cs} \pm \Delta V_{Cs}$	V	56.9 ± 997m	0.21 ± 999m	56.7 ± 999m	0.122 ± 1.00
ave $I_{Ls} \pm \Delta I_{Ls}$	V	1.328 ± 145m	1.330 ± 145m	1.328 ± 145m	1.330 ± 145m
$V_o \pm \Delta V_o$	V	57.18 ± 54µ	57.18 ± 0.1	57.17 ± 9µ	57.19 ± 0.1
P_{out}	W	76.21	76.21	76.17	76.23
efficiency η	%	95.38	95.27	95.32	95.27

The open-loop simulation results in Figure 4, summarized in table 4, albeit at the same operating point for all four converters, confirm that the ac operating conditions are identical. The differences are in the split-capacitor dc bias and the ripple in the input current (discontinuous/ discontinuous) and output voltage ripple, due to discontinuous output current. The low output voltage ripple for the Cuk and zeta converters, because of continuous output current, illustrates that the 100uF output capacitance C_o could be reduced. Nonetheless, output capacitor equivalent series resistance, ESR, not accounted for in the simulations, would tend to dominate the output ripple voltage. Generally, the small simulation variations are due to the different Joule losses in the various operating Kirchhoff voltage loops.

VI. EXPERIMENTAL RESULTS

Figure 3 illustrates that all four split-capacitor converters can be practically assessed with a single hardware arrangement, with facilities to reconnect the transformer winding terminations. With the transformer winding terminal connected to the each of the split capacitors fixed, the output voltage polarity is fixed, independent of the connection (0V or E_i / V_o) of the remaining winding terminals. Also, Figure 7 will show that the same commonality exists for the

necessary switch leakage energy clamping snubber circuit.

Since no mmf bias is required of the coupling transformer, the high relative permeability (>30,000) and high saturation flux density >1.2T, of low-loss, high Curie temperature, nanocrystalline strip core material can be exploited, with switching frequencies in excess of 100kHz. The high permeability justifies the high transformer magnetizing inductance (100mH:100mH) used in the simulations.

Experimental results are open loop. Because the ac circuit is identical for all four converters, the 408W practical result in Figure 5 is indistinguishable between the four converters, including the overshoot and ringing components. The RCD snubber uses ½nF of capacitance, amounting to 0.05W of loss (at E_i=20Vdc and 50kHz); which is insignificant to the overall converter efficiency.

Differences (36.2W in 408W) between simulated and experimental results in Figure 5 are accounted for by non-modeled core losses, winding proximity and eddy (Foucault) current created copper losses, plus switching and RCD snubber losses that are not modeled.

VII. SUMMARY OF PRACTICAL RESULTS

Figure 6 shows the open-loop dependence of capacitor voltage and ripple, output voltage and current regulation (droop), and efficiency, on average input current magnitude I_i. The converter circuit component values are as shown in Table 3. Without exception, these graphs show that the ac characteristics of the four converters are indistinguishable, expected given all four have the same ac equivalent circuit. Any differences are due to losses in the output capacitor due to different ripple currents, hence ESR I^2R losses.

The efficiency and voltage regulation deteriorate (near linearly) with increased load/input current. In confirming the inductor ripple current equations in Table 2 and equations (11) and (12), the inductor ripple currents are independent of load current - figures 4 and 5. Figure 6c shows that converter efficiency decreases with load.

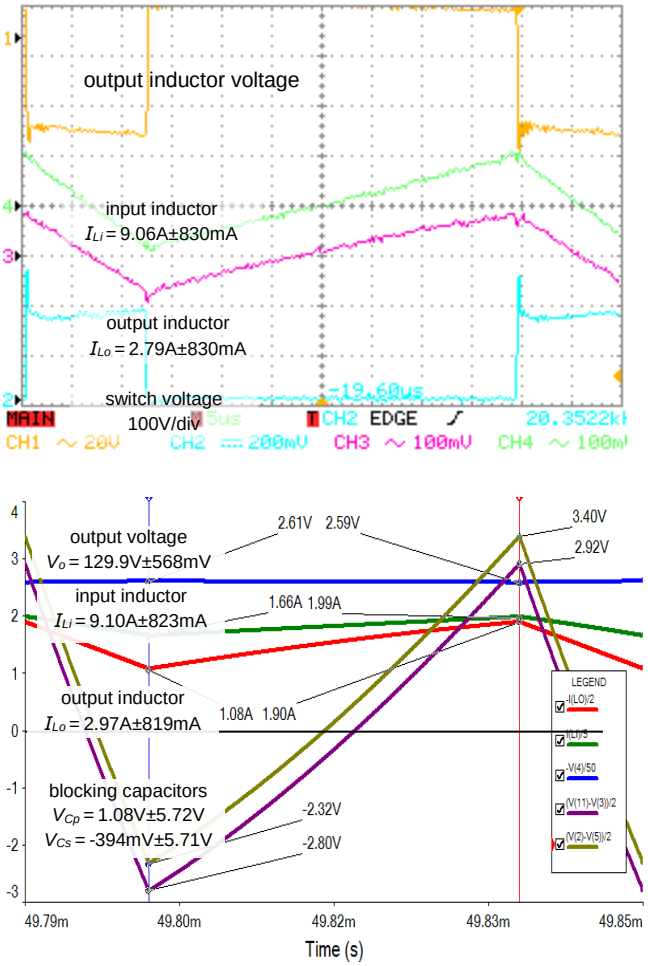

Fig .5. Simulation and experimental results for the transformer coupled buck-boost converter P5, at 20kHz, 45Vdc, 9A ave (408W) input, η = 85.7% (output 125.3Vdc, 2.79A).

Also in accordance with the theory, equations (2) and (3) and table II, the capacitor ripple voltage Δv_c in Figure 6(d) increases linearly with increased load current (for a given δ, etc.) and is independent of terminal input/output voltages. Due to circuit Kirchhoff loop losses, specifically the unequal inductor resistive component voltages, not included in the theory, the capacitors have a current-dependant small dc bias (in addition to any input/output dc blocking voltage), which is duty cycle and load dependant, as shown in Figure 6(a). Figures 4 and 5 show that if the inductances are equal ($L_i = L_o$), with a transformer 1:1 turns ratio, the ripple current magnitudes are equal. From Table I, the relative average current magnitudes in both inductor windings (which equal the average input/output currents), change-over at δ=½, when V_o=E_i.

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In contrast to the poor open-loop output voltage regulation, the converters exhibit good output current regulation characteristics, as shown in Figure 6(b). The voltage regulation in Figure 6(b) deteriorates because semiconductor voltages and *IR* drops detract from the effective input and output voltages. On the other hand, the current transfer ratio is largely unaffected by voltage components; it is purely a relation between the input and output current, independent of the input voltage. Hence, at the modest input voltage of 20V dc, the current regulation is significantly better than the voltage regulation. Such a regulation feature is common to all dc-to-dc converters.

Increasing the input voltage from 20V dc to 30V dc to 45V dc, for a given input current results in improved efficiency (as shown in Figure 4c), hence better voltage regulation, since the Joule *IR* type voltage drops become less significant. For example, at 8A average input current, the efficiency increases from 73% to 75.5%, corresponding to the open-loop output voltage droop decreasing from 26% to 16.5%, for 20V dc and 30V dc, respectively. As shown in Figure 5 and plotted in Figure 6, the efficiency at 45Vdc and 9A average input improves to 85.7%, at 20kHz. Switch RCD snubber losses at a few tens of milliwatts, are insignificant.

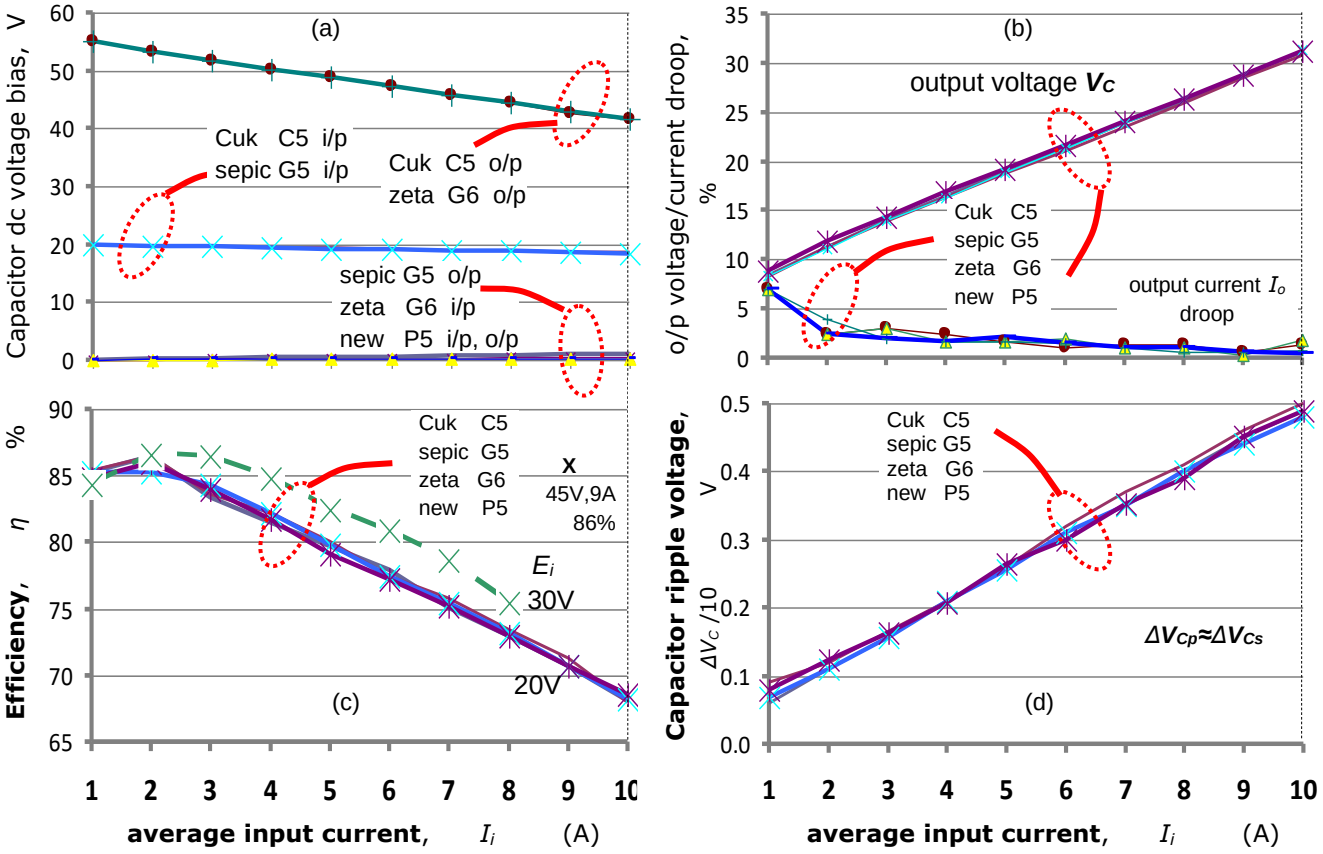

Fig .6. Experimental results at 50kHz, δ=75%, E_i = 20V and varied average input current, for the four transformer-coupled buck-boost dc-to-dc converters (C5≡Cuk, G5≡sepic, G6≡zeta, P5≡New): (a) capacitor C_p and C_s dc voltage bias, (b) output voltage V_o and current I_o regulation (droop), (c) efficiency, and (d) capacitor C_p and C_s ripple voltage/10.

VIII. OPERATIONAL CONSTRAINTS

Each circuit configuration (coupled and uncoupled) has leakage and/or stray inductance, hence it suffers from trapped energy switch and diode over voltage at commutation. The key physical design aspect is to minimize stray/leakage inductance, accomplished by using transformer bifilar windings and a core with as high as possible permeability (low core reluctance). Since stray/leakage inductance inevitably remains, current commutation overlap occurs, whence switch turn-on snubbering is inherent. Switch/diode turn-off clamping/snubber energy if not dissipated, any energy recovered should feed back to the supply rather than the output, which is variable, so as not to affect the output regulation and more importantly not to upset

the transformer Vμs balance, which is hyper-critical in single-switch converter configurations, if core saturation is to be avoided.

The inevitable leakage in itself is not a problem, nor is a high converter power rating. Converter topology physical construction and electrical isolation are similar up to about 1kV. That is, leakage and stray inductance are largely independent of voltage up to 1kV. Trapped energy is determined by the current magnitude, squared. Thus, the lower the voltage for a given power rating, the higher the current, which results in significantly higher trapped energy being proportional to current squared $½LI^2$. Therefore, low-voltage high-current converter design is challenging. A single power semiconductor clamping device (5W transient voltage suppressor) but not a metal oxide voltage suppressor (high capacitive energies at high frequencies) is adequate for a few Watts of losses, as shown in Figure 7(a). At higher dissipation levels, an RCD snubber as shown in Figure 7(b), not only controls inductive leakage current induced voltage levels, but also reduces switch turn-off losses. At even higher current levels, the complication of snubber energy recovery may be viable, where active techniques are required, as shown in figures 7(c) and 7(d). The switch T_r in Figure 7(c) is self synchronized, its gate being ac coupled via an auxiliary auto-transformer winding on L_i. The main switch T and recovery switch T_r are gated together, and the topology in Figure 7(d).i can use a common gate driver (with T_r gate ac coupled as in Figure 7(c)). The minimum reset time (minimum switch on-time), $t_{on} \geq t_1 + t_2$, comprises a fixed period $t_1 = ½\pi/\omega_o$ where $\omega_o = \sqrt{L_r C_{sn}}$, at which time the snubber capacitor retains zero voltage, provided $\eta_{Xc} < ½ V_{Csn\ max}/E_i$. The interval t_2 is source voltage and trapped energy dependant ($V_{Csn\ max}$), specifically $t_2 = (V_{Csn\ max} - \eta_{Xc} E_i) / \eta_{Xc} \omega_o E_i$, where η_{Xc} is the reset transformer turns ratio, effectively ηXc is unity for Figure 7(c) analysis.

The leakage energy associated with the recovery transformer in Figure 7(d), is also recovered, and the series inductance L_r function may be fulfilled by recovery transformer leakage. The same snubber topology is employed on the switch/diode on both sides of the transformer, which then also caters for bidirectional converter operation.

Attempts at passive energy recovery are hampered since the switch supporting voltage V_o+E_i is more than the supply voltage E_i but less than the peak voltage $V_{Csn\ max}$, produced by capacitor storage of the trapped energy.

Previous active recovery circuits [25] use a floating switch gate/source, that experiences high *dv/dt*'s. Also the main switch experiences the recovery current at switch turn-on [25] and energy is fed into the output circuit, which is a variable voltage; therefore portion of the reset period is not only load current dependant but also duty cycle dependant [25].

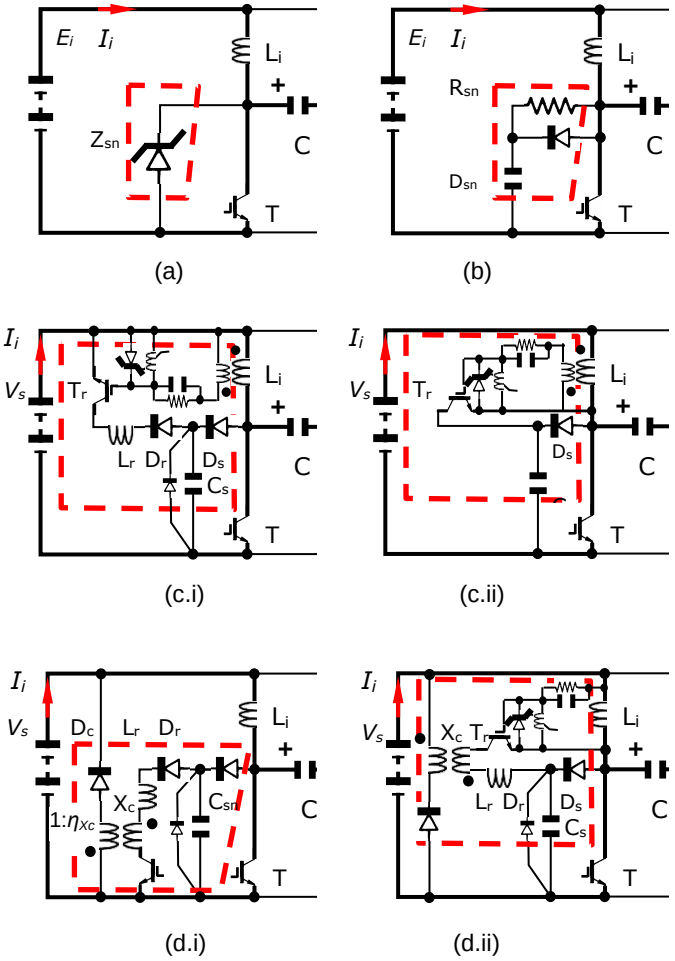

Fig .7. Stray/leakage inductance energy clamping techniques: (a) Zener clamp, $V_z > E_i+V_o$, (b) RCD/soft clamp snubber, (c) active regenerative turn-off snubber, and (d) isolated active recovery.

IX. CONCLUSIONS

Four single-switch, transformer-coupled buck–boost converters have been analyzed and assessed theoretically, in simulation and experimentally. This paper has highlighted the ac circuit equivalence of the Cuk, sepic, zeta and new converters. All four converters use two inductors and two split mirroring capacitors with a shunt transformer interposed, and

have identical ac characteristics, but differ in terms of mirroring capacitor dc bias. The external input and output ac current conditions differ, being combinations of either continuous and/or discontinuous. The voltage transfer function is independent of inductor ripple current, being dependant on average inductor currents. Specifically, the primary-side inductor average current is the average input current, while the secondary-side inductor average current is the average output current, in the ratio $\delta/(1-\delta)$, independent of current ripple. Discontinuous conduction is inductor ripple current magnitude dependant, while capacitor constant voltage mode characteristics (capacitor equivalent to inductor DCM) are induced by inductor DCM (and vice versa).

The transformer dc current (hence flux) bias in the conventionally coupled sepic and zeta converters under utilizes the core two quadrant flux swing capability and increases the total copper losses. The copper losses are increased because of the reduced allowable flux swing, and with an air gap the number of turns for a given inductance increases, hence resistance increases. By separating transformer and inductor functions, each can be optimally and independently designed.

Practically, the only limitation in realizing a high-power single-switch, transformer-isolated dc-to-dc converter, is trapped energy associated with stray and leakage inductances. Four clamping/snubber circuits, to cater for the leakage trapped energy at switch turn-off, have been proposed, which facilitate operation from a few watts output to over 2kW.

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