Investigation of Efficiency and Thermal Performance of the Y-source Converters for a Wide Voltage Range

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Abstract - The Y-source topology has a unique advantage of having high voltages gain with small shoot through duty cycles. Furthermore, having the advantage of high modulation index increases the power density and improves the performance of the converter. In this paper, a collective thermal and efficiency investigation is performed in order to improve the reliability of the converter. Losses evaluation in the semiconductor devices (switching/conduction), the capacitors (ESR), and the inductors (core/winding) are presented. Moreover, the junction temperature evaluation of the devices is considered under 25◦ C ambient temperature. The analysis is carried out at the following voltages gain (2, 3, and 4), and at the following winding factors (4, and 5) using PLECS toolbox. The results show that, the power losses and the junction temperature are directly proportional with the voltage gain and the winding factor.

Keywords – Y-Source Converter-core losses-winding losses-Thermal-Voltage gain-Duty cycle.

I. INTRODUCTION

Y-source power converter has been used in many renewable energy applications such as; renewable generation systems [1], fuel cell applications [2], and more recently with electric vehicles [3]. Due to the importance of the thermal behaviour from the reliability point of view, a collective investigation of efficiency and thermal performance has to be done for the Y-source converter. Unreasonable temperature during the operation of the converter affects the performance, the devices lifetime, and hence, the reliability of the power electronic components in the converter. Therefore, controlling the tempera- ture within the reasonable limits provides: 1- higher power densities. 2- lower cost system configuration. 3- reliability improvement from lifetime point of view. 4- increase of the overall efficiency of the converter. 5- insuring safety and preventing the catastrophic design mistakes.

Practical applications require high switching frequency with small shoot through cycles to reduce the power losses during the turn-on and turn-off transients. For a short duration, a high current passes through the switch causing high voltage stress and high junction temperature. Moreover, having higher voltages gain increases the stress in the device which needs to be designed carefully. Thus, it is very important to consider the thermal challenges earlier in the design stage. Considering these challenges improves the performance of the converter by protecting the devices to be exposed to excessive temperatures that shorten their lifetime [4], and hence, the reliability of the converter.

This paper aims to investigate the thermal performance of the Y-source converter operating under 500 W at switching frequency of 20 kHz [5], [6], and [7]. The investigation is considered at voltages gain (2, 3, and 4), and at winding factors (4, and 5). The main sections in this paper are as follows: Section II gives the topology of the Y-source converter and its theory of operation. Section III illustrates the calculations of the efficiency and losses. Section IV presents the simulated case studies. Section V presents the simulation results and discussion, followed by the conclusion.

II. TOPLOGY AND THEORY OF OPERATION

The Y-source converter is a very promising topology for higher voltage gain in a small duty ratio and in a very wide range of adjusting the voltage gain [6]. Very high modulation index can be achieved with this topology as well. The range of duty cycle in the Y-source is narrower than Z-source and the boost and higher in the modulation index. Fig.1 (a) shows the Y-source impedance network is realized a three-winding coupled inductor (N1, N2, and N3) for introducing the high boost at a small duty ratio for SW. It has an active switch SW, passive diodes (D1,

D2), a capacitor C1, the windings of the coupled inductor are connected directly to SW and D1, to ensure very small leakage inductances at its winding terminals.

- In the ST state, when the switch is turned on, D1 and D2 are off causing the capacitor C1 to charge the magnetizing inductor of the coupled transformer and capacitor C2 discharge to power the load.

- In the NST state, when the switch is non-conducting,D1 starts to conduct causing the input voltage to recharge the capacitor C1 and the energy from the supply and the transformer to flow to the load and when D2 starts

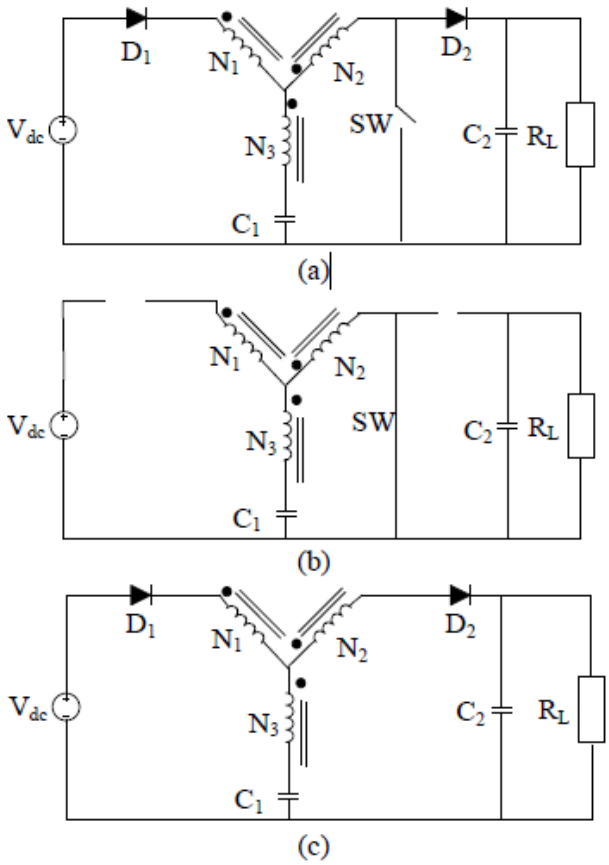

Fig .1. Illustration of a)Y-source converter, b) its equivalent "ST state", and c) its equivalent "NST state" circuits..

conducting, it recharges C2 and the load to be continuously powered.

The input /output voltage relation and the duty cycle isexpressed in (1)

$$V_{out} = \frac{V_{in}}{(1 - KD)} \quad (1)$$

where, V_{out} is the output voltage, V_{in} is the input voltage, D is the duty cycle and K is the winding factor.

The winding factor K is calculated according to the turns ratio of the three-winding coupled inductor as expressed in (2)

$$K = \frac{N_1 + N_3}{N_3 - N_2} \quad (2)$$

where, (N_1 : N_2 : N_3) is the turns ratio of the coupled inductor.

And the modulation index M of the Y-source is expressed in (3)

$$M = 1.15\,(1 - D) \quad (3)$$

where, D is the duty cycle required for the voltage gain and M is the modulation index.

III. EFFICINCY AND LOSS CALCULATIONS

In this section, further illustration for the formulas used in calculating the relevant losses and verified by the simulation results. Having passive elements in the Y-source circuit, may have some advantages as 1) minimizing the stresses according to the desired design, 2) reduceing the switching and conduction losses on the devices, 3) lowering shoot through duration, since they are storing energy.

A. Switching and conduction losses calculations

Switching losses occurs when the device is transitioning from the blocking state to the conducting state and vice-versa. This interval is characterized by a significant voltage across its terminals and a significant current through it. The energy dissipated in each transition needs to be multiplied by the frequency to obtain the switching losses:

The switching losses P_{sw} are expressed in (4):

$$P_{sw} = (E_{on} + E_{off}) \times f_{sw} \quad (4)$$

Where, E_{on} and E_{off} are the energy losses during on and off of the switch, f_{sw} is the switching frequency. Conduction losses occurs when the device is in full conduction. The current in the device is whatever is

required by the circuit and the voltage at its terminals is the voltage drop due to the device itself. These losses are in direct relationship with the duty cycle.

The average conduction losses P_{cond} are expressed in (5):

$$P_{avg.cond} = \frac{1}{T}\int_0^T [v_{ce}(t) \times i_{ce}(t)]\, dt \quad (5)$$

where, v_{ce} is the on state voltage, an i_{ce} is the on state current. And in (6):

$$T = \frac{1}{f_{sw}} \quad (6)$$

B. Capacitor ESR losses calculations

The Equivalent Series Resistance ESR is the value of resistance which is equal to the total effect of a large set of energy loss mechanisms occurring under the operating conditions. So, the capacitors losses are expressed in (7):

$$P_{cap.loss} = I^2_{cap.} \times ESR \quad (7)$$

where, $I_{cap.}$ is the rms current passing through the capacitor, and ESR is the equivalent series resistance measuring the effect of the losses dissipated in the capacitor.

C. Winding and core losses calculations

According to Steinmetz's equation [8], which is a physics equation used to calculate the core loss of magnetic materials due to magnetic hysteresis.

The core losses are expressed in (8):

$$P_v = k f^{\alpha} \hat{B}^{\beta} \quad (8)$$

Where, Bˆ is the peak induction of a sinusoidal excitation on the efficiency and junction temperature performances. Furthermore, measuring all the relevant losses as listed in section with frequency f, P_v is the time-average power loss per unit volume, and the material parameters (α, β, k) are material parameters.

The improved generalized Steinmetz's equation is expressed in (9):

$$P = \frac{1}{T}\int_0^T k_i \left|\frac{dB}{dt}\right|^a (\Delta B^{b-a})\, dt \quad (9)$$

Where, ΔB is the flux density from peak to peak and in (10):

$$k_i = \frac{k}{(2\pi)^{\alpha-1}\int_0^{2\pi} |cos\theta|^{\alpha} \times 2^{\beta-\alpha} d\theta} \quad (10)$$

Where, *(β, α, k)* are the material parameter found by curve fitting, and *θ* is the angle of the sinusoidal waveform simulated.

IV. CASE STUDIES

In this section, simulations are carried out to verify the performance of the Y-source converter using the parameters listed in Table I.

Table 1. THE USED PARAMETERS OF THE SIMULATED MODEL.

Parameters	Values / Models
Input voltage V_{in}	100 V - 133 V - 200 V
Output voltage V_o	400 V
Output Power P_o	500 W
Switching frequency f_s	20 kHz
Resistive load R_l	320 Ω
MOSFET SW	SPW47N60C3 650 V, 47 A
Diode $D_1 - D_2$	SD600N/R 600 V, 600 A
Core type V	MPP C055863A2

Table 2. SIMULATION PARAMETERS AT THREE CASES.

Parameters	Values
Size of AWG	15
Winding factor K	4 5
Turns ratio $N_1 : N_2 : N_3$	80:16:48 48:16:32
DC-resistance $R_{dc-Y\ source}$	0.0735 Ω 0.0441Ω
	0.0147 Ω 0.0147Ω
	0.0441 Ω 0.0294Ω

The ratings of the devices are chosen according to the voltage and current stresses across them. Where, investigating the impact of varying the voltage gain and the winding factor on the efficiency and junction temperature performances. Fur- thermore, measuring all the relevant losses as listed in section While having the same switching frequency 20 kHz, rated power 500 W, and constant ambient temperature 25 ◦C. Table II summarize the case studies investigated.

- Case 1:

Simulation was carried out with voltage gain factor 2 with different value of shoot-through ratio, using winding factors 4 and 5. The rated power 500 W was applied to all the simulations.

- Case 2:

Simulation was carried out with voltage gain factor 3 with different value of shoot-through ratio, using winding factors 4 and 5.

- Case 3:

Simulation was carried out with voltage gain factor 4 with different value of shoot-through ratio, using winding factors 4 and 5.

V. SIMULATION RESULTS AND DISSCUSION

PLECS toolbox is used for the Y-source converter circuit. All the relevant losses results are calculated based on the afore-mentioned equations in the simulated model. The simulated parameters are listed in Table II. Where, the comparison is between 2 different winding factors (4, and 5), and 3 different voltage gains (2, 3, and 4), the size of the wire is 15 AWG and the values of the DC resistance are calculated according to 11:

$$R_{dc} = R_{dc/singlelayer} \times \frac{N}{L} \quad (11)$$

Where, ($R_{dc/singlelayer}$) is the dc resistance per single layer, N is the no. of turns, and L is the length of single layer.

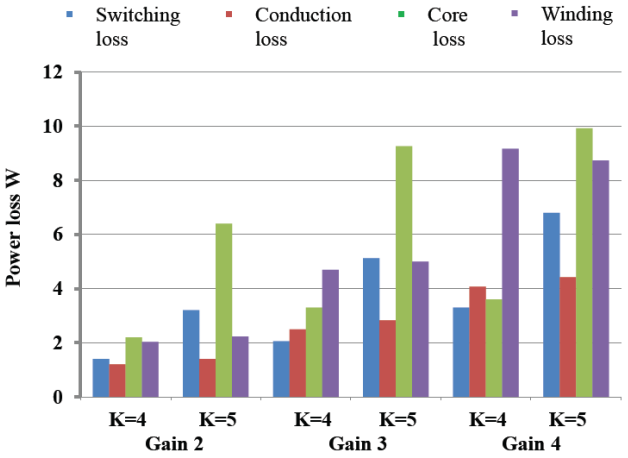

Fig .2. Representation of the relevant losses for cases I, II, and III.

Table 3. THE SIMULATED SHOOT-THROUGH DUTY CYCLE FOR EACH CASE.

Cases	Gain	Winding factor *K*		Duty cycle *D*	
Case I	2	4	5	0.125	0.1
Case II	3	4	5	0.16674	0.133
Case III	4	4	5	0.18754	0.15

Table 4. THE SIMULATED SHOOT-THROUGH DUTY CYCLE FOR EACH CASE.

Cases	Winding factor *K*		Total power losses *W*		Efficiency %	
Case I - Gain 2	4	5	6.93	13.19	98.61	97.48
Case II - Gain 3	4	5	12.6	22.2	97.5	95.8
Case III - Gain 4	4	5	20.2	29.9	96.1	94.4

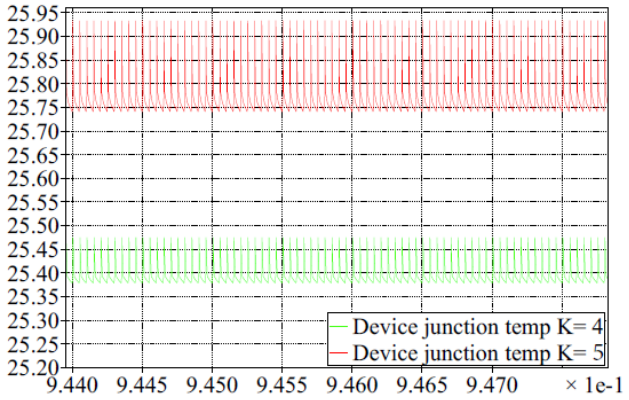

Fig .2 Junction temperation representation at gain 2 for K= 4 and K= 5.

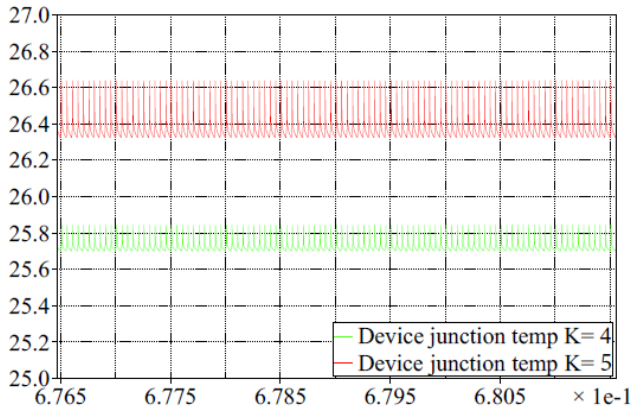

Fig .4 Junction temperation representation at gain 2 for K= 4 and K= 5.

Fig. 2 presents the difference between the relevant losses of the devices (switching, conduction, core and winding losses) for each winding factor and voltage gain. For the capacitor ESR losses, it can be neglected, since it is very small where, the largest is 0.26 watts at gain 4 and winding factor 5. For the shoot through duty ratios for each case is listed in Table III. The simulation results indicate that the higher the voltage gain and winding factor, the higher the power losses and the junction temperature which are listed in Table IV. For the junction temperature variation in the MOSFET for different gains and winding factors in steady state, Figures 3, 4 and 5 that show the behaviour of the junction temperature under different voltage gains and winding factors. The highest junction temperature is at voltage gain factor of 4 and winding factor of 5 as expected.

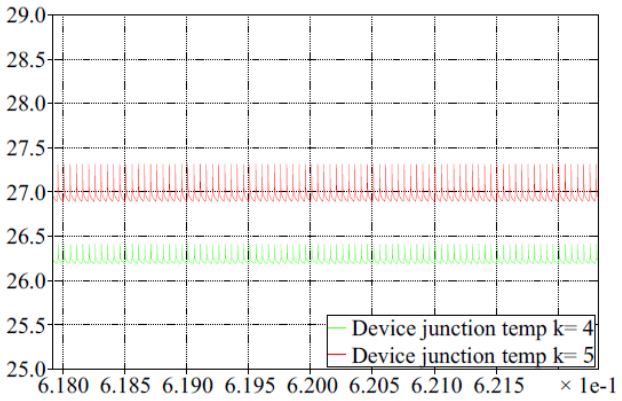

Fig .5 Junction temperation representation at gain 4 for K= 4 and K= 5.

VI. CONCLUSIONS

This paper investigates the thermal performance and the efficiency of semiconductor devices and passive elements in the Y-source converter of rated power 500 W. In sake of designing a reliable converter, the thermal performance is extremely important to be considered. Measurements of the junction temperatures and relevant losses are demonstrated. The impact of different voltage gains and winding factors is performed and studied. The measurements of the junction temperature variation shows that there is no overstress on the devices during the operation, this is due to the unique advantage in the Y-source converter of having high voltage gains with very small duty ratio. The results of the relevant losses with respect to varying the voltage gains and winding factor are reasonable. It can be seen from the results that while increasing the voltage gains and the winding factors, the total power loss increase as well. The performance of the Y-source converter is very promising. Although having voltage gain factor of 4, the performance is efficient and the converter's efficiency is ranging between 94.4 % and 96 % with respect to the winding factor variation.

REFERENCES

[1] J.-M. Shen, H.-L. Jou, and J.-C. Wu, "Ripple voltage suppression method for dc/dc boost converter of the grid- connected renewable power generation system," in IEEE International Conference on Sustainable Energy Technolo- gies, 2008. ICSET 2008., Nov 2008, pp. 110–115.

[2] Y. Siwakoti, F. Z. Peng, F. Blaabjerg, P. C. Loh, and G. Town, "Impedance-source networks for electric power conversion part i: A topological review," IEEE Transac- tions on Power Electronics, vol. 30, no. 2, pp.

699–716, Feb 2015.

[3] O. Hegazy, J. Van Mierlo, and P. Lataire, “Analysis, control and comparison of dc/dc boost converter topolo- gies for fuel cell hybrid electric vehicle applications,” in Proceedings of the 2011-14th European Conference on Power Electronics and Applications (EPE 2011), Aug 2011, pp. 1–10.

[4] A. K. Chanudhary, S. K. Singh, S. Singh, and F. Ahmed, “Reliability tests and thermal modelling for inverter in hy- brid electrical vehicles,” International Journal of Scientific Technology Research, vol. 1, no. 4, pp. 1–5, May 2012.

[5] Y. Siwakoti, G. Town, P. C. Loh, and F. Blaabjerg, “Y- source inverter,” in IEEE 5th International Symposium on Power Electronics for Distributed Generation Systems (PEDG), 2014, June 2014, pp. 1–6.

[6] Y. Siwakoti, P. C. Loh, F. Blaabjerg, and G. Town, “Y- source impedance network,” in 2014 Twenty-Ninth Annual IEEE Applied Power Electronics Conference and Exposi- tion (APEC),, March 2014, pp. 3362–3366.

[7] Y. Siwakoti, P. C. Loh, F. Blaabjerg, S. Andreasen, and G. Town, “Y-source boost dc/dc converter for distributed generation,” IEEE Transactions on Industrial Electronics,, vol. 62, no. 2, pp. 1059–1069, Feb 2015.

[8] J. Muhlethaler, J. Biela, J. Kolar, and A. Ecklebe, “Core losses under the dc bias condition based on steinmetz parameters,” IEEE Transactions on Power Electronics, vol. 27, no. 2, pp. 953–963, Feb 2012.